Patent claims

1. An electronic component comprising the following features:

- a stack (2) of semiconductor chips (3, 4), having
  - a first semiconductor chip (3) and
  - a stacked second semiconductor chip (4), the semiconductor chips (3, 4) having an active upper face (5) with contact pads (6) to integrated circuits and a rear face (7)
- a flat conductor structure (8) comprising
  - a chip island (9),
  - flat conductors (10) which surround the chip island (9), and
  - contact pillars (11) which are arranged on the flat conductors (10) and are aligned orthogonally with respect to the flat conductors (10),

wherein the second semiconductor chip (4) is arranged with its rear face (7) on the chip island (9) and wherein its contact pads (6) are electrically connected via bonding wire connections (12) to the flat conductors (10), and wherein the first semiconductor chip (3) is surrounded by the contact pillars (11) and is arranged underneath the chip island (9) in such a way that pillar contact pads (13) of the contact pillars (11), upper face areas (14) of a plastic encapsulation compound (15) which embeds the semiconductor chips (3, 4), the contact pillars (11) and the flat conductor structure (8), and the active upper face (5) of the first semiconductor chip (3), form an overall upper face (16), and wherein a wiring layer (17) is arranged on the overall upper face (16) and electrically connects the semiconductor chips (3, 4) to one another via wiring lines (18).

2. The electronic component as claimed in claim 1, characterized in that
the wiring layer (17) comprises a wiring level (19)

which is arranged on the overall upper face (16) and comprises outer contact pads (20), which are electrically connected via the wiring lines (18) to the pillar contact pads (13) of the contact pillars (11), and/or to the contact pads (6) on the first semiconductor chip (3).

3. The electronic component as claimed in claim 1 or claim 2,
characterized in that
solder balls (21) are arranged on the outer contact pads (20).

4. A panel which comprises a leadframe (22) with electronic components (1) of one of claims 1 to 3, the electronic components (1) being arranged in rows and columns.

5. The panel as claimed in claim 4,
characterized in that the shape of the panel (23) corresponds in its extent and extent markings to a standard semiconductor wafer.

6. A method for production of a panel (23) for a plurality of electronic components (1), wherein the method comprises the following method steps:

- production of a leadframe (22) with component positions (24) arranged in rows and columns, whereby a component position (24) comprises a chip island (9) and flat conductors (10) which surround the chip island (9), as well as contact pillars (11), which are arranged on the flat conductors (10) and are aligned orthogonally with respect to the flat conductors (10),
- application of a stacked semiconductor chip (4) to the chip island (9) of the component positions (24),
- production of bonding wire connections (12)

between the flat conductors (10) and contact pads (6) on active upper faces (5) of the stacked semiconductor chips (3, 4),

- application of first semiconductor chips (3) with their active upper faces (5) to a carrier (25) with adhesive bonding on one side, with the first semiconductor chips (3) being arranged in rows and columns which correspond to the rows and columns of the component positions (24),
- application of the leadframe (22) with stacked semiconductor chips (4) to the carrier (25) in such a way that the contact pillars (11) of the leadframe (22) are adhesively bonded by their upper faces to the carrier (25) and the first semiconductor chips (3) are arranged on the carrier (25) underneath the chip islands (9) of the leadframe (22) and are surrounded by contact pillars (11),
- embedding of the leadframe (22) with stacked semiconductor chips (3, 4) and bonding wire connections (12) in a plastic compound (26) to form a composite body (27) on the carrier (25),
- removal of the carrier (25) exposing an overall upper face (16) composed of active upper faces (5) of the first semiconductor chips (3), pillar contact pads (13) of the contact pillars (11), and an upper face (14) of the plastic compound (26),
- application of a wiring layer (17) to the overall upper face (16), forming wiring lines (18) and outer contact pads (20),

wherein the wiring lines (18) connect the outer contact pads (20) to the contact pads (6) of the first semiconductor chip (3), and/or to the pillar contact pads (13) of the contact pillars (11).

7. The method as claimed in claim 6,
characterized in that
solder balls (21) are applied to the outer contact pads

(20) to provide outer contacts.

8. A method for production of an electronic component, comprising the following method steps:

- production of a panel (23) as claimed in claim 6 or claim 7,
- separation of the panel (23) into individual electronic components (1).

9. The method as claimed in claim 8, characterized in that outer contacts are applied to the outer contact pads (20) of an electronic component (1).